Embedded Wafer Level System Integration

Amkor Technology Portugal (formerly Nanium) was among the first in the world to offer Wafer Level Fan-Out (WLFO) packaging, enabling a wide range of embedded heterogeneous system integration package solutions, such as Wafer Level System-in-Package (WLSiP) a single or multiple die, with or without passives or sensors integration and 3D Package Stacking solutions (WL3D), including Wafer Level Package-on-Package and Face-to-Face package assembly.

Tailoring the best solutions requires a deep understanding of customer needs. Amkor’s package solutions are collaboratively developed, which often involves cooperation from the earliest stage of the Chip-Package-Board co-design. Amkor is recognized for its proficiency in advanced packaging, and is known for a portfolio of innovative solutions manufactured in volume. These include the largest reliable WLCSP to date.

By relying on an experienced in-house R&D team to design and develop innovative package and system solutions for a wide range of applications, we enable products from concept to market.

As a leader in wafer-level packaging, Amkor offers world-class, turnkey solutions on state-of-the-art 300 mm wafer-processing equipment. In addition, we consistently deliver the best results in key metrics such as time to market, cost efficiency and yield.

Advanced Packaging Solutions

- WLSiP side-by-side multi-chip modules
- WLSiP with passives and leadless package integration
- Portfolio of WLSiP ranges from 2 x 3 mm² (2 components) to 33 x 28 mm² (10 components)
- WL3D Package-on-Package by stacking WLSiP and other package types using Through Package Vias (TPV)
- 3D integration by F2F assembly of Flip Chip to WLFO package

Cross-Sections – WLFO-based Embedded Wafer Level System Integration Portfolio

WLSiP Passives Integration

WLSiP Multi-Chip Module

WL3D Face-to-Face

WL3D RDL on Both Sides Through Package Vias

WLSiP Multi-Chip Module

WL3D Package-on-Package, Face-to-Face, Through Package Vias
WLSiP and WL3D Packaging

Design Features
- Package size 2 x 3 mm² - 33 x 28 mm²
- Package thickness 0.275 mm (WLSiP – Multi-Chip Module) to 1.900 mm (WL3D)
- WLSiP with up to 10 active dies and 50 passives qualified
- Minimum Through Package Via (TPV) pitch 0.350 mm
- BGA pitch down to 0.350 μm
- Min die-to-die distance 0.100 mm
- Min passive-to-die and passive-to-passive distance 0.150 mm
- Min die TV pad pitch 0.050 mm and opening 0.045 mm
- Bottom side Cu-RDL min line/space 0.010 mm/0.010 mm, multi-layer RDL
- Top side Cu-RDL min line/space 0.020 mm/0.020 mm, single-layer RDL

Differentiation
- High integration density through small die-to-die distance
- Multi-layer RDL and double-sided RDL (WLFO bottom and top side)
- 3D stacking enabled by TPV concept
- Small form-factor (optimization based on customer needs in footprint or z-height)
- BGA ball attach and Flip Chip with underfill assembly on same WLFO bottom side
- Heterogeneous integration of multiple different active dies (Si, GaAs, SiGe), already packaged dies, passives, optical elements, sensors and MEMS

Reliability: Board Level Tests
With a wide range of different WLSiP and WL3D package constructions and configurations possible, customer requirements are implemented in each product developed and reliability results are realized based on technical capabilities.

<table>
<thead>
<tr>
<th>Test</th>
<th>Specification</th>
<th>Criteria</th>
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</thead>
<tbody>
<tr>
<td><strong>Lower Complexity WLSiP</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Cycling on Board (TCoB)</td>
<td>IPC-9701 condition TC3</td>
<td>-40°C/+125°C, 1cy/hr</td>
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<tr>
<td>Drop Test (DT)</td>
<td>JEDEC JESD-22-B111</td>
<td>100 drops</td>
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<tr>
<td><strong>Higher Complexity WL3D</strong></td>
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<tr>
<td>Temperature Cycling on Board (TCoB)</td>
<td>IPC-9701 condition TC3</td>
<td>-40°C/+125°C, 1cy/hr</td>
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<tr>
<td>Drop Test (DT)</td>
<td>JEDEC JESD-22-B111</td>
<td>30 drops</td>
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<tr>
<td>Temperature Humidity Bias (THB)</td>
<td>JEDEC JESD-22-A101</td>
<td>85°C/85%rH/Vcc</td>
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</tbody>
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