Technology Solutions

Fan-Out Wafer Level Packaging

Wafer-Level System-in-Package (WLSiP) and Package-on-Package (PoP)

Wafer-Level Packaging applies similar processes as used in front-end wafer processing. One advantage is the batch processing, where all components on a large wafer format are efficiently processed simultaneously.

Today, “More than Moore”, heterogeneous integration of different elements in package level and embedded technologies is the trend. Reducing the form factor while increasing the number of IOs is necessary to integrate more functionality in the system. Fan-Out WLP is the answer to those challenges. It allows system integration at the wafer-level with the highest integration density.

Amkor is licensed for Fan-Out WLP technology eWLB (embedded Wafer Level Ball Grid Array) and is one of the technology drivers in this new packaging technology platform. Together with its partner, Amkor developed the 300 mm reconstituted wafer solution, ramping this technology into high volume manufacturing. As of today, 500 million eWLB components have been shipped.

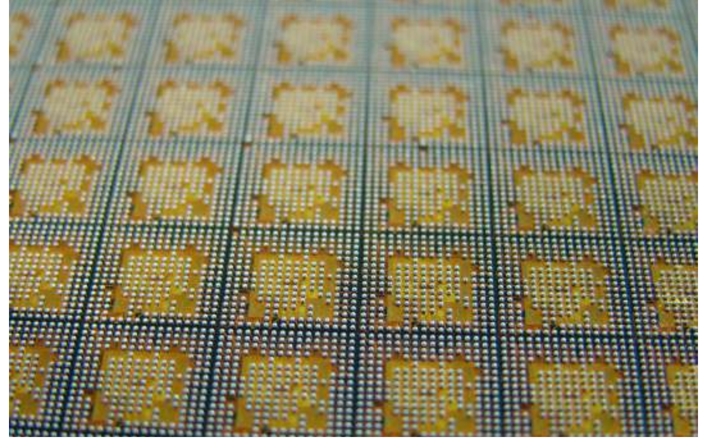
Applications

- Mobile and consumer products, baseband, RF, analog, power management
- ASIC, MEMS, system solutions for medical, security, encryption, DC/DC converter, radar
- Electro-Optical WLSiP, solutions for M2M Communication and the “Internet of Everything”
- Extension of the technology platform to a wider field of application areas is ongoing

Design Features

- Chip-first approach with KGD from probed front-end wafers
- Supports all kinds of incoming wafer diameter and chip packaging media
- Reconstituted wafer (chip embedding in epoxy)
- Single die and multi die solutions, possibility of embedded discrete passives
- Package size: from below 1 x 1 mm² to 12 x 12 mm² (up to 25 x 25 mm² under development)

Bumped Wafer



Dispensed Mold Compound

- Package thickness: 0.3-1.0 mm
- Single-layer RDL
- Double sided RDL for PoP applications under development
- Several UBM types for improved reliability
- BGA bump pitch down to 0.400 mm (down to 0.300 mm under development)
- Bare die backside for heat spreader assembly, overmold or backside coating by tape
- Standard laser marking and packing

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Differentiation

- Chip size independent package design with small package size adder
- High degree of package design freedom, fan-out zone adaptable to customer needs
- No restrictions in bump pitch, covering IO gap between IC and PCB
- No laminate substrate required, shorter interconnections, excellent electrical performance
- Lower thermal resistance compared to FCiP and conventional substrate based BGA
- System-in-Package on Wafer-Level (WLSiP) and Package-on-Package (PoP) Solutions
- Smaller footprint and thinner package than FCiP BGA, no need for underfill
- Reliable, miniaturized high performance package
- RoHS and REACH compliant package
- Cost effective due to 300 mm wafer batch processing and no need of extra interposer
- Highly simplified supply chain and manufacturing infrastructure
- Better board level reliability and backside protection compared to WLCSP

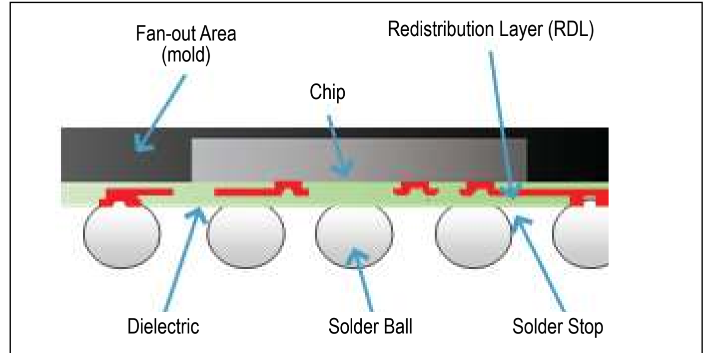
Fan-Out Wafer Level Packaging Performance Data: Reliability

Component Level Tests

(9.25 x 8.80 mm², Single Die, 1L-Cu-RDL, no UBM, 222 bumps, 0.400 mm pitch)

Test	Specification	Criteria
Moisture Sensitivity Level (MSL)	EIA/J-STD-020C Level 1	MSL1 for lead free (260°C peak temperature)
Temperature Cycling Test (TCT)	JEDEC JESD-22-A104 Condition B	-55°C/125°C 1500x
High Temperature Storage (HTS)	JEDEC JESD-22-A103	150°C 1000h
Unbiased HAST (µHAST)	JEDEC JESD-22-A118 Condition A	130°C/85%rH 186h
Temperature Humidity Bias (THB)	JEDEC JESD-22-A101	85°C/85%rH/Vcc 1000h

Cross Section



Board Level Tests

(9.25 x 8.80 mm², Single Die, 1L-Cu-RDL, no UBM, 222 bumps, 0.400 mm pitch)

Test	Specification	Criteria
Temperature Cycling on Board (TCoB)	IPC-97-01	-40°C/125°C - 1 cy/hr 1000x
Temperature Cycling on Board (TCoB)	Customer Spec	-40°C/125°C - 2 cy/hr >500x
Drop Test	JEDEC JESD-22-B111	FF > 150 drops
Drop Test	Customer Spec	<10% fails @ 20 drops

Thermal

Strongly dependent on chip size to package size ratio, RDL line width and thickness, number and position of I/Os, type of backside protection.

Example for reference: Package size 8 x 8 mm, chip size 5 x 5 mm shows thermal performance Rth junction-ambient = 32.5 K/W and Rth junction-case = 6.5 K/W

Electrical

Excellent performance data compared to conventional wirebonded BGA and FCiP with significantly reduced package parasitics:

Interconnect Level	BGA	FCiP	eWLB
Resistance @ DC [mO]	76	7.5	3.2
Resistance @ 5 GHz [mO]	375	41	15
Inductance [nH]	1.100	0.052	0.018
Package Level	**BGA**	**FCiP**	**eWLB**
Resistance @ DC [mO]	89	22	23
Resistance @ 5 GHz [mO]	629	248	91
Inductance [nH]	1.790	0.950	0.340

*Due to the very low inductance values, this package type is excellent for high speed applications, such as RF and Radar, proven up to 81 GHz.

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